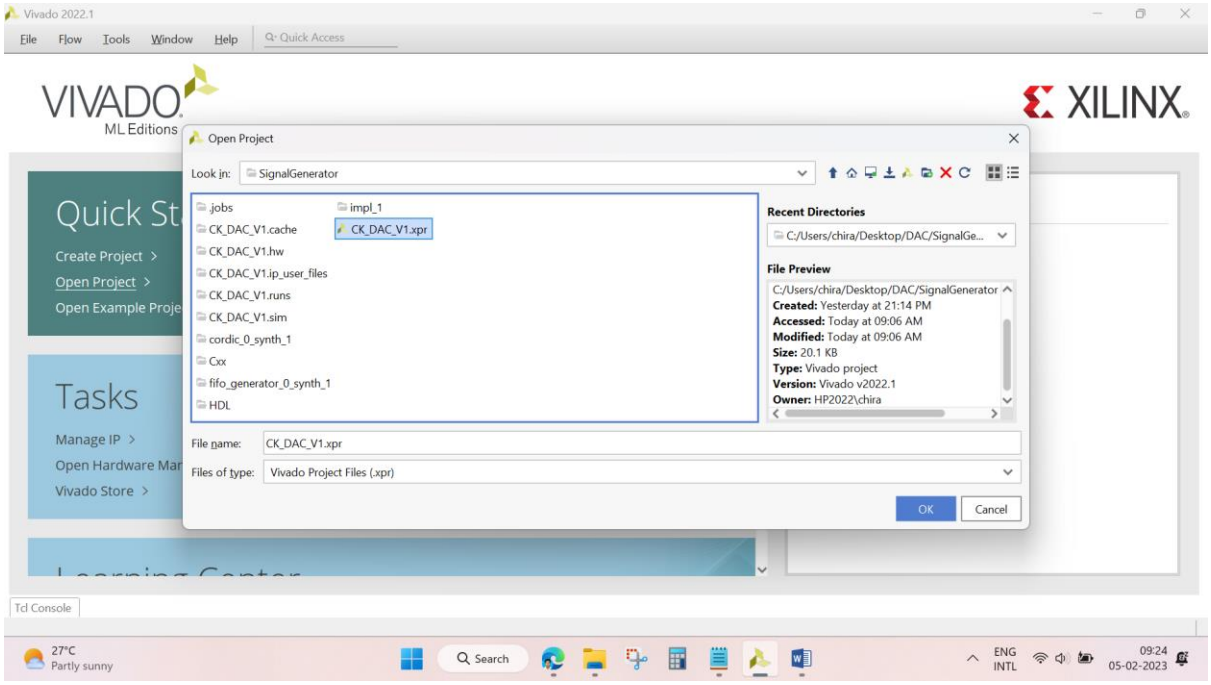
I have **XEM8320 and SZG-DAC-AD911X** is a dual 125 MSPS DAC, that I am trying to build a simple project with the help of the files from **SYZYGYfpga/xem7320-syzygy-samples.**

I have followed the procedure as mentioned in 'Readme'. The same is here for ready reference;

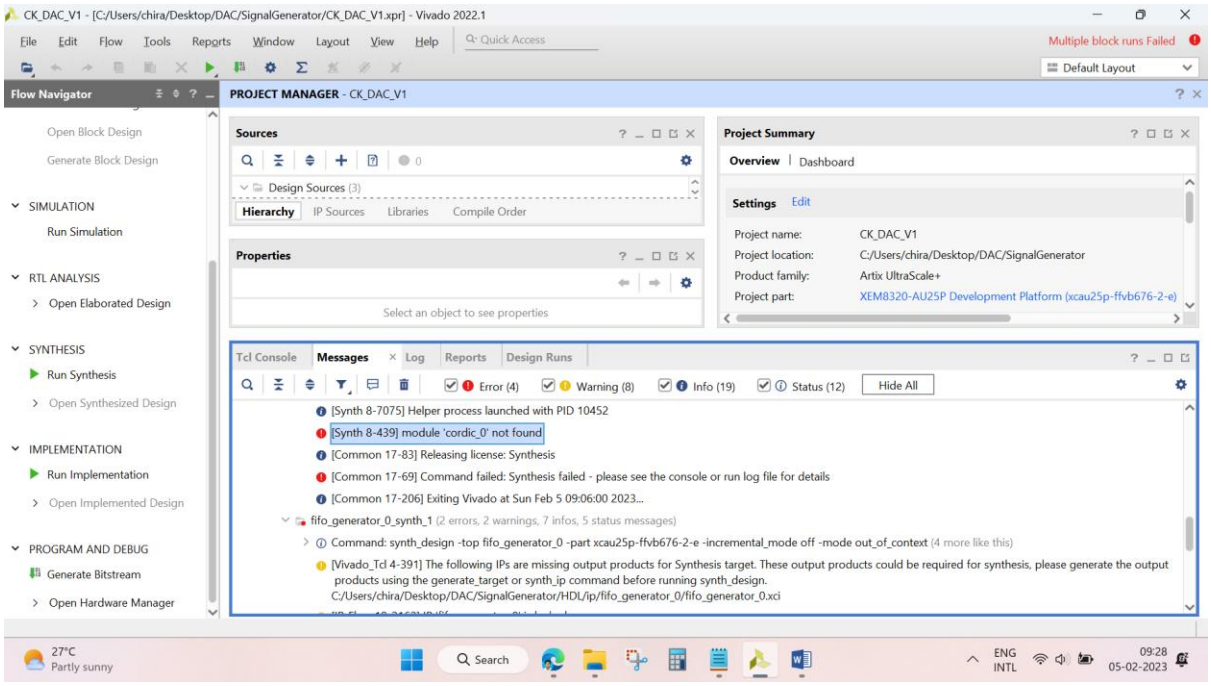
"To build each sample design, start a new Vivado project with the xc7a75tfgg484-1 part selected and add the sources in the HDL folder to the project. With the project created and sources added, simply click the "Generate Bitstream"."

I have created a new project in **Vivado 2022.1**, which has preinstalled **ArtixUltrascale+ and KintexUltrascale+ and the XEM8320 board files**.

From there I have selected the XEM8320 board and created the project with name **CK_DAC_V1**, and placed it in the same directory of the "SignalGenerator". For reference a screen picture is given below after the system failed to run.



The error message that has been generated after the click on *Generate Bitstream; is given below.*

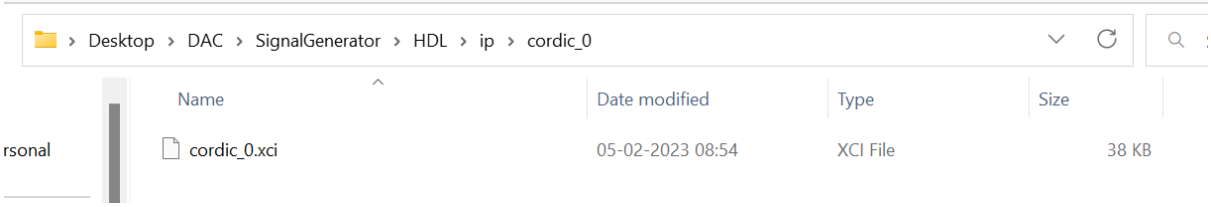


The detail message log is placed in the Table.pdf (attached).

The basic errors are **module 'cordic_0'** and **module 'fifo_generator_0'** not found.

Tracking cordic_0 error; following are the submission.

The cordic_0.xic is placed here;



The generated cordic_0 related files are here;