```
set_property CFGBVS GND [current_design]
set_property CONFIG_VOLTAGE 1.8 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS True [current_design]

##############################################################################
## FrontPanel Host Interface
##############################################################################
set_property PACKAGE_PIN U20 [get_ports {okHU[0]}]
set_property PACKAGE_PIN U26 [get_ports {okHU[1]}]
set_property PACKAGE_PIN T22 [get_ports {okHU[2]}]
set_property SLEW FAST [get_ports {okHU[*]}]
set_property IOSTANDARD LVCMOS18 [get_ports {okHU[*]}]

set_property PACKAGE_PIN V23 [get_ports {okUH[0]}]
set_property PACKAGE_PIN T23 [get_ports {okUH[1]}]
set_property PACKAGE_PIN U22 [get_ports {okUH[2]}]
set_property PACKAGE_PIN U25 [get_ports {okUH[3]}]
set_property PACKAGE_PIN U21 [get_ports {okUH[4]}]
set_property IOSTANDARD LVCMOS18 [get_ports {okUH[*]}]

set_property PACKAGE_PIN P26 [get_ports {okUHU[0]}]
set_property PACKAGE_PIN P25 [get_ports {okUHU[1]}]
set_property PACKAGE_PIN R26 [get_ports {okUHU[2]}]
set_property PACKAGE_PIN R25 [get_ports {okUHU[3]}]
set_property PACKAGE_PIN R23 [get_ports {okUHU[4]}]
set_property PACKAGE_PIN R22 [get_ports {okUHU[5]}]
set_property PACKAGE_PIN P21 [get_ports {okUHU[6]}]
set_property PACKAGE_PIN P20 [get_ports {okUHU[7]}]
set_property PACKAGE_PIN R21 [get_ports {okUHU[8]}]
set_property PACKAGE_PIN R20 [get_ports {okUHU[9]}]
set_property PACKAGE_PIN P23 [get_ports {okUHU[10]}]
```

```
set_property PACKAGE_PIN N23 [get_ports {okUHU[11]}]
set_property PACKAGE_PIN T25 [get_ports {okUHU[12]}]
set_property PACKAGE_PIN N24 [get_ports {okUHU[13]}]
set_property PACKAGE_PIN N22 [get_ports {okUHU[14]}]
set_property PACKAGE_PIN V26 [get_ports {okUHU[15]}]
set_property PACKAGE_PIN N19 [get_ports {okUHU[16]}]
set_property PACKAGE_PIN V21 [get_ports {okUHU[17]}]
set_property PACKAGE_PIN N21 [get_ports {okUHU[18]}]
set_property PACKAGE_PIN W20 [get_ports {okUHU[19]}]
set_property PACKAGE_PIN W26 [get_ports {okUHU[20]}]
set_property PACKAGE_PIN W19 [get_ports {okUHU[21]}]
set_property PACKAGE_PIN Y25 [get_ports {okUHU[22]}]
set_property PACKAGE_PIN Y26 [get_ports {okUHU[23]}]
set_property PACKAGE_PIN Y22 [get_ports {okUHU[24]}]
set_property PACKAGE_PIN V22 [get_ports {okUHU[25]}]
set_property PACKAGE_PIN W21 [get_ports {okUHU[26]}]
set_property PACKAGE_PIN AA23 [get_ports {okUHU[27]}]
set_property PACKAGE_PIN Y23 [get_ports {okUHU[28]}]
set_property PACKAGE_PIN AA24 [get_ports {okUHU[29]}]
set_property PACKAGE_PIN W25 [get_ports {okUHU[30]}]
set_property PACKAGE_PIN AA25 [get_ports {okUHU[31]}]
set_property SLEW FAST [get_ports {okUHU[*]}]
set_property IOSTANDARD LVCMOS18 [get_ports {okUHU[*]}]

set_property PACKAGE_PIN T19 [get_ports okAA]
set_property IOSTANDARD LVCMOS18 [get_ports okAA]

create_clock -period 9.920 -name okUH0 [get_ports {okUH[0]}]

set_input_delay -clock [get_clocks okUH0] -max -add_delay 8.000 [get_ports {okUH[*]}]
set_input_delay -clock [get_clocks okUH0] -min -add_delay 9.920 [get_ports {okUH[*]}]
```

```
#set_multicycle_path -setup -from [get_ports {okUH[*]}] 2

set_input_delay -clock [get_clocks okUH0] -max -add_delay 7.000 [get_ports {okUHU[*]}]
set_input_delay -clock [get_clocks okUH0] -min -add_delay 2.000 [get_ports {okUHU[*]}]
#set_multicycle_path -setup -from [get_ports {okUHU[*]}] 2

set_output_delay -clock [get_clocks okUH0] -max -add_delay 2.000 [get_ports {okHU[*]}]
set_output_delay -clock [get_clocks okUH0] -min -add_delay -0.500 [get_ports {okHU[*]}]

set_output_delay -clock [get_clocks okUH0] -max -add_delay 2.000 [get_ports {okUHU[*]}]
set_output_delay -clock [get_clocks okUH0] -min -add_delay -0.500 [get_ports {okUHU[*]}]

##############################################################################
## System Clock
##############################################################################
set_property IOSTANDARD LVDS [get_ports sys_clkp]

set_property PACKAGE_PIN T24 [get_ports sys_clkp]
set_property PACKAGE_PIN U24 [get_ports sys_clkn]
set_property IOSTANDARD LVDS [get_ports sys_clkn]

create_clock -period 10.000 -name sys_clk [get_ports sys_clkp]
set_clock_groups -asynchronous -group [get_clocks sys_clk] -group [get_clocks {mmcm0_clk0 okUH0}]
set_property CLOCK_DEDICATED_ROUTE BACKBONE [get_nets idelay_adc_enc_clk/inst/clk_in1_clk_wiz_0]

# LEDS ########################################################################
set_property PACKAGE_PIN G19 [get_ports {led[0]}]
set_property PACKAGE_PIN B16 [get_ports {led[1]}]
set_property PACKAGE_PIN F22 [get_ports {led[2]}]
set_property PACKAGE_PIN E22 [get_ports {led[3]}]
```

```
set_property PACKAGE_PIN M24 [get_ports {led[4]}]
set_property PACKAGE_PIN G22 [get_ports {led[5]}]
set_property IOSTANDARD LVCMOS18 [get_ports {led[*]}]

############################################################
# ADC Section - PORT A
############################################################

# PORTA-5
set_property PACKAGE_PIN L18 [get_ports {adc_out_1p_pA[0]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_1p_pA[0]}]

# PORTA-6
set_property PACKAGE_PIN M25 [get_ports adc_fr_p_pA]
set_property IOSTANDARD LVDS [get_ports adc_fr_p_pA]

# PORTA-7
set_property PACKAGE_PIN K18 [get_ports {adc_out_1n_pA[0]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_1n_pA[0]}]

# PORTA-8
set_property PACKAGE_PIN M26 [get_ports adc_fr_n_pA]
set_property IOSTANDARD LVDS [get_ports adc_fr_n_pA]

# PORTA-9
set_property PACKAGE_PIN M20 [get_ports {adc_out_1p_pA[1]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_1p_pA[1]}]

# PORTA-10
set_property PACKAGE_PIN L24 [get_ports {adc_out_2p_pA[0]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_2p_pA[0]}]
```

```
# PORTA-11
set_property PACKAGE_PIN M21 [get_ports {adc_out_1n_pA[1]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_1n_pA[1]}]

# PORTA-12
set_property PACKAGE_PIN L25 [get_ports {adc_out_2n_pA[0]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_2n_pA[0]}]

# PORTA-14
set_property PACKAGE_PIN K25 [get_ports {adc_out_2p_pA[1]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_2p_pA[1]}]

# PORTA-16
set_property PACKAGE_PIN K26 [get_ports {adc_out_2n_pA[1]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_2n_pA[1]}]

# PORTA-33
set_property PACKAGE_PIN J23 [get_ports adc_dco_p_pA]
set_property IOSTANDARD LVDS [get_ports adc_dco_p_pA]

# PORTA-34
set_property PACKAGE_PIN H26 [get_ports adc_encode_p_pA]
set_property IOSTANDARD LVDS [get_ports adc_encode_p_pA]

# PORTA-35
set_property PACKAGE_PIN J24 [get_ports adc_dco_n_pA]
set_property IOSTANDARD LVDS [get_ports adc_dco_n_pA]

# PORTA-36
set_property PACKAGE_PIN G26 [get_ports adc_encode_n_pA]
```

```
set_property IOSTANDARD LVDS [get_ports adc_encode_n_pA]


# ADC timing constraints

create_clock -period 2.000 -name adc_dco_p_pA -waveform {0.000 1.000} [get_ports adc_dco_p_pA]

set_input_delay -clock [get_clocks adc_dco_p_pA] -clock_fall -min -add_delay .350 [get_ports {adc_out_1p_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -clock_fall -max -add_delay .650 [get_ports {adc_out_1p_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -min -add_delay .350 [get_ports {adc_out_1p_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -max -add_delay .650 [get_ports {adc_out_1p_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -clock_fall -min -add_delay .350 [get_ports {adc_out_1n_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -clock_fall -max -add_delay .650 [get_ports {adc_out_1n_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -min -add_delay .350 [get_ports {adc_out_1n_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -max -add_delay .650 [get_ports {adc_out_1n_pA[*]}]


set_input_delay -clock [get_clocks adc_dco_p_pA] -clock_fall -min -add_delay .350 [get_ports {adc_out_2p_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -clock_fall -max -add_delay .650 [get_ports {adc_out_2p_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -min -add_delay .350 [get_ports {adc_out_2p_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -max -add_delay .650 [get_ports {adc_out_2p_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -clock_fall -min -add_delay .350 [get_ports {adc_out_2n_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -clock_fall -max -add_delay .650 [get_ports {adc_out_2n_pA[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -min -add_delay .350 [get_ports {adc_out_2n_pA[*]}]
```

```
set_input_delay -clock [get_clocks adc_dco_p_pA] -max -add_delay .650 [get_ports {adc_out_2n_pA[*]}]


set_input_delay -clock [get_clocks adc_dco_p_pA] -clock_fall -min -add_delay .350 [get_ports {adc_fr_p_pA}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -clock_fall -max -add_delay .650 [get_ports {adc_fr_p_pA}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -min -add_delay .350 [get_ports {adc_fr_p_pA}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -max -add_delay .650 [get_ports {adc_fr_p_pA}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -clock_fall -min -add_delay .350 [get_ports {adc_fr_n_pA}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -clock_fall -max -add_delay .650 [get_ports {adc_fr_n_pA}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -min -add_delay .350 [get_ports {adc_fr_n_pA}]

set_input_delay -clock [get_clocks adc_dco_p_pA] -max -add_delay .650 [get_ports {adc_fr_n_pA}]


set_clock_groups -name decode_reset_group -asynchronous -group [get_clocks -of_objects [get_pins okHI/mmcm0/CLKOUT0]] -group [get_clocks -include_generated_clocks adc_dco_p_pA]

set_property CLOCK_DEDICATED_ROUTE BACKBONE [get_nets adc_impl_portA/adc_dco_impl_portA/clk_out_int_BUFG]


############################################################

# ADC Section - PORT B

############################################################


# PORTB-5

set_property PACKAGE_PIN A22 [get_ports {adc_out_1p_pB[0]}]

set_property IOSTANDARD LVDS [get_ports {adc_out_1p_pB[0]}]


# PORTB-6

set_property PACKAGE_PIN A24 [get_ports adc_fr_p_pB]

set_property IOSTANDARD LVDS [get_ports adc_fr_p_pB]
```

```
# PORTB-7
set_property PACKAGE_PIN A23 [get_ports {adc_out_1n_pB[0]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_1n_pB[0]}]

# PORTB-8
set_property PACKAGE_PIN A25 [get_ports adc_fr_n_pB]
set_property IOSTANDARD LVDS [get_ports adc_fr_n_pB]

# PORTB-9
set_property PACKAGE_PIN E21 [get_ports {adc_out_1p_pB[1]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_1p_pB[1]}]

# PORTB-10
set_property PACKAGE_PIN D24 [get_ports {adc_out_2p_pB[0]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_2p_pB[0]}]

# PORTB-11
set_property PACKAGE_PIN D21 [get_ports {adc_out_1n_pB[1]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_1n_pB[1]}]

# PORTB-12
set_property PACKAGE_PIN D25 [get_ports {adc_out_2n_pB[0]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_2n_pB[0]}]

# PORTB-14
set_property PACKAGE_PIN C23 [get_ports {adc_out_2p_pB[1]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_2p_pB[1]}]

# PORTB-16
set_property PACKAGE_PIN B24 [get_ports {adc_out_2n_pB[1]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_2n_pB[1]}]
```

```
# PORTB-33
set_property PACKAGE_PIN G24 [get_ports adc_dco_p_pB]
set_property IOSTANDARD LVDS [get_ports adc_dco_p_pB]

# PORTB-34
set_property PACKAGE_PIN H21 [get_ports adc_encode_p_pB]
set_property IOSTANDARD LVDS [get_ports adc_encode_p_pB]

# PORTB-35
set_property PACKAGE_PIN G25 [get_ports adc_dco_n_pB]
set_property IOSTANDARD LVDS [get_ports adc_dco_n_pB]

# PORTB-36
set_property PACKAGE_PIN H22 [get_ports adc_encode_n_pB]
set_property IOSTANDARD LVDS [get_ports adc_encode_n_pB]

# ADC timing constraints
create_clock -period 2.000 -name adc_dco_p_pB -waveform {0.000 1.000} [get_ports
adc_dco_p_pB]
set_input_delay -clock [get_clocks adc_dco_p_pB] -clock_fall -min -add_delay .350 [get_ports
{adc_out_1p_pB[*]}]
set_input_delay -clock [get_clocks adc_dco_p_pB] -clock_fall -max -add_delay .650 [get_ports
{adc_out_1p_pB[*]}]
set_input_delay -clock [get_clocks adc_dco_p_pB] -min -add_delay .350 [get_ports
{adc_out_1p_pB[*]}]
set_input_delay -clock [get_clocks adc_dco_p_pB] -max -add_delay .650 [get_ports
{adc_out_1p_pB[*]}]
set_input_delay -clock [get_clocks adc_dco_p_pB] -clock_fall -min -add_delay .350 [get_ports
{adc_out_1n_pB[*]}]
set_input_delay -clock [get_clocks adc_dco_p_pB] -clock_fall -max -add_delay .650 [get_ports
{adc_out_1n_pB[*]}]
set_input_delay -clock [get_clocks adc_dco_p_pB] -min -add_delay .350 [get_ports
{adc_out_1n_pB[*]}]
```

```
set_input_delay -clock [get_clocks adc_dco_p_pB] -max -add_delay .650 [get_ports {adc_out_1n_pB[*]}]


set_input_delay -clock [get_clocks adc_dco_p_pB] -clock_fall -min -add_delay .350 [get_ports {adc_out_2p_pB[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -clock_fall -max -add_delay .650 [get_ports {adc_out_2p_pB[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -min -add_delay .350 [get_ports {adc_out_2p_pB[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -max -add_delay .650 [get_ports {adc_out_2p_pB[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -clock_fall -min -add_delay .350 [get_ports {adc_out_2n_pB[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -clock_fall -max -add_delay .650 [get_ports {adc_out_2n_pB[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -min -add_delay .350 [get_ports {adc_out_2n_pB[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -max -add_delay .650 [get_ports {adc_out_2n_pB[*]}]


set_input_delay -clock [get_clocks adc_dco_p_pB] -clock_fall -min -add_delay .350 [get_ports {adc_fr_p_pB}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -clock_fall -max -add_delay .650 [get_ports {adc_fr_p_pB}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -min -add_delay .350 [get_ports {adc_fr_p_pB}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -max -add_delay .650 [get_ports {adc_fr_p_pB}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -clock_fall -min -add_delay .350 [get_ports {adc_fr_n_pB}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -clock_fall -max -add_delay .650 [get_ports {adc_fr_n_pB}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -min -add_delay .350 [get_ports {adc_fr_n_pB}]

set_input_delay -clock [get_clocks adc_dco_p_pB] -max -add_delay .650 [get_ports {adc_fr_n_pB}]


set_clock_groups -name decode_reset_group -asynchronous -group [get_clocks -of_objects [get_pins okHI/mmcm0/CLKOUT0]] -group [get_clocks -include_generated_clocks adc_dco_p_pB]
```

```
set_property CLOCK_DEDICATED_ROUTE BACKBONE [get_nets
adc_impl_portB/adc_dco_impl_portB/clk_out_int_BUFG]

############################################################

# ADC Section - PORT C

############################################################

# PORTC-5

set_property PACKAGE_PIN F20 [get_ports {adc_out_1p_pC[0]}]

set_property IOSTANDARD LVDS [get_ports {adc_out_1p_pC[0]}]

# PORTC-6

set_property PACKAGE_PIN C18 [get_ports adc_fr_p_pC]

set_property IOSTANDARD LVDS [get_ports adc_fr_p_pC]

# PORTC-7

set_property PACKAGE_PIN E20 [get_ports {adc_out_1n_pC[0]}]

set_property IOSTANDARD LVDS [get_ports {adc_out_1n_pC[0]}]

# PORTC-8

set_property PACKAGE_PIN C19 [get_ports adc_fr_n_pC]

set_property IOSTANDARD LVDS [get_ports adc_fr_n_pC]

# PORTC-9

set_property PACKAGE_PIN H18 [get_ports {adc_out_1p_pC[1]}]

set_property IOSTANDARD LVDS [get_ports {adc_out_1p_pC[1]}]

# PORTC-10

set_property PACKAGE_PIN H17 [get_ports {adc_out_2p_pC[0]}]

set_property IOSTANDARD LVDS [get_ports {adc_out_2p_pC[0]}]
```

```
# PORTC-11
set_property PACKAGE_PIN H19 [get_ports {adc_out_1n_pC[1]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_1n_pC[1]}]

# PORTC-12
set_property PACKAGE_PIN G17 [get_ports {adc_out_2n_pC[0]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_2n_pC[0]}]

# PORTC-13
#set_property PACKAGE_PIN F18 [get_ports adc_sdo_1]
#set_property IOSTANDARD LVCMOS18 [get_ports adc_sdo_1]

# PORTC-14
set_property PACKAGE_PIN A17 [get_ports {adc_out_2p_pC[1]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_2p_pC[1]}]

# PORTC-15
#set_property PACKAGE_PIN F19 [get_ports adc_cs_2n]
#set_property IOSTANDARD LVCMOS18 [get_ports adc_cs_2n]

# PORTC-16
set_property PACKAGE_PIN A18 [get_ports {adc_out_2n_pC[1]}]
set_property IOSTANDARD LVDS [get_ports {adc_out_2n_pC[1]}]

# PORTC-17
#set_property PACKAGE_PIN E16 [get_ports adc_sck_2]
#set_property IOSTANDARD LVCMOS18 [get_ports adc_sck_2]

# PORTC-19
#set_property PACKAGE_PIN E17 [get_ports adc_sdi_2]
#set_property IOSTANDARD LVCMOS18 [get_ports adc_sdi_2]
```

```
# PORTC-33
set_property PACKAGE_PIN E18 [get_ports adc_dco_p_pC]
set_property IOSTANDARD LVDS [get_ports adc_dco_p_pC]

# PORTC-34
set_property PACKAGE_PIN C17 [get_ports adc_encode_p_pC]
set_property IOSTANDARD LVDS [get_ports adc_encode_p_pC]

# PORTC-35
set_property PACKAGE_PIN D18 [get_ports adc_dco_n_pC]
set_property IOSTANDARD LVDS [get_ports adc_dco_n_pC]

# PORTC-36
set_property PACKAGE_PIN B17 [get_ports adc_encode_n_pC]
set_property IOSTANDARD LVDS [get_ports adc_encode_n_pC]


# ADC timing constraints
# ADC timing constraints
create_clock -period 2.000 -name adc_dco_pC -waveform {0.000 1.000} [get_ports adc_dco_p_pC]
set_input_delay -clock [get_clocks adc_dco_p_pC] -clock_fall -min -add_delay .350 [get_ports {adc_out_1p_pC[*]}]
set_input_delay -clock [get_clocks adc_dco_p_pC] -clock_fall -max -add_delay .650 [get_ports {adc_out_1p_pC[*]}]
set_input_delay -clock [get_clocks adc_dco_p_pC] -min -add_delay .350 [get_ports {adc_out_1p_pC[*]}]
set_input_delay -clock [get_clocks adc_dco_p_pC] -max -add_delay .650 [get_ports {adc_out_1p_pC[*]}]
set_input_delay -clock [get_clocks adc_dco_p_pC] -clock_fall -min -add_delay .350 [get_ports {adc_out_1n_pC[*]}]
set_input_delay -clock [get_clocks adc_dco_p_pC] -clock_fall -max -add_delay .650 [get_ports {adc_out_1n_pC[*]}]
```

```
set_input_delay -clock [get_clocks adc_dco_p_pC] -min -add_delay .350 [get_ports {adc_out_1n_pC[*]}]

set_input_delay -clock [get_clocks adc_dco_pC] -max -add_delay .650 [get_ports {adc_out_1n_pC[*]}]


set_input_delay -clock [get_clocks adc_dco_p_pC] -clock_fall -min -add_delay .350 [get_ports {adc_out_2p_pC[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -clock_fall -max -add_delay .650 [get_ports {adc_out_2p_pC[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -min -add_delay .350 [get_ports {adc_out_2p_pC[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -max -add_delay .650 [get_ports {adc_out_2p_pC[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -clock_fall -min -add_delay .350 [get_ports {adc_out_2n_pC[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -clock_fall -max -add_delay .650 [get_ports {adc_out_2n_pC[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -min -add_delay .350 [get_ports {adc_out_2n_pC[*]}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -max -add_delay .650 [get_ports {adc_out_2n_pC[*]}]


set_input_delay -clock [get_clocks adc_dco_p_pC] -clock_fall -min -add_delay .350 [get_ports {adc_fr_p_pC}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -clock_fall -max -add_delay .650 [get_ports {adc_fr_p_pC}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -min -add_delay .350 [get_ports {adc_fr_p_pC}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -max -add_delay .650 [get_ports {adc_fr_p_pC}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -clock_fall -min -add_delay .350 [get_ports {adc_fr_n_pC}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -clock_fall -max -add_delay .650 [get_ports {adc_fr_n_pC}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -min -add_delay .350 [get_ports {adc_fr_n_pC}]

set_input_delay -clock [get_clocks adc_dco_p_pC] -max -add_delay .650 [get_ports {adc_fr_n_pC}]
```

```
set_clock_groups -name decode_reset_group -asynchronous -group [get_clocks -of_objects [get_pins okHI/mmcm0/CLKOUT0]] -group [get_clocks -include_generated_clocks adc_dco_p_pC]
```